

Communicating with AcubeSAT via a SatNOGS based platform

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AcubeSAT is a 3U CubeSat, developed to conduct a biological experiment in Low Earth Orbit (LEO), designed and built by the interdisciplinary volunteering student team SpaceDot, at the Aristotle University of Thessaloniki. Aiming to investigate how gene expression in eukaryotic cells is dynamically regulated in space, this satellite is designed to record their growth and provide valuable experimental data, via its onboard imaging system, to the Ground Station. By demonstrating a novel payload design for high-throughput life sciences' studies in orbit, AcubeSAT presents demanding requirements in terms of communication resources.

After the successful environmental qualification campaign of the Communications (COMMS) Board based on the Libre Space Foundation (LSF) SatNOGS COMMS board design, conducted with the support of the Fly Your Satellite! 3 programme at ESA Academy's testing facilities, the communications team is now advancing towards the development of networking applications for AcubeSAT. A complete end-to-end network architecture is being implemented, spanning from the Ground Station to the application layer software running onboard, utilizing open source tools for the Mission Control Software, such as YAMCS. Although the mission poses significant technical challenges, progress in the development of the physical layer has been advancing steadily, by implementing the modulation and demodulation techniques, as well as the encoding and decoding methods on the flight software and hardware.

This presentation aims to highlight the current status of AcubeSAT's communications subsystem while also providing a deeper dive into its physical layer. A closer look at the in-house developed Offset Quadrature Phase-Shift Keying (OQPSK) modulator, used for high-speed transactions between the mission's terminals to transfer experiment results, will offer insight into both the GNU Radio tool developed for the Ground Station and the corresponding Field Programmable Gate Array (FPGA) Intellectual Property (IP) Core.

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